查询CMP401供应商

23 ns and 65 ns Low Voltage Comparators

CMP401/CMP402

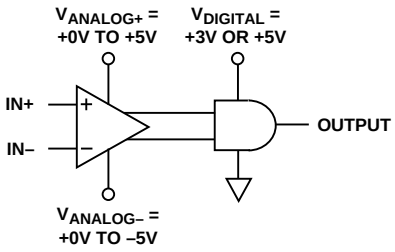
FEATURES

23 ns or 65 ns Propagation Delay
Single-Supply Operation
Compatible with +3 V and +5 V Logic
Separate Input and Output Sections
Low Power
Wide Input Range: –5 V to +3.9 V

APPLICATIONS

Battery Operated Instrumentation
Line Receivers
Level Translators
Read Channel Detection

FUNCTIONAL BLOCK DIAGRAM

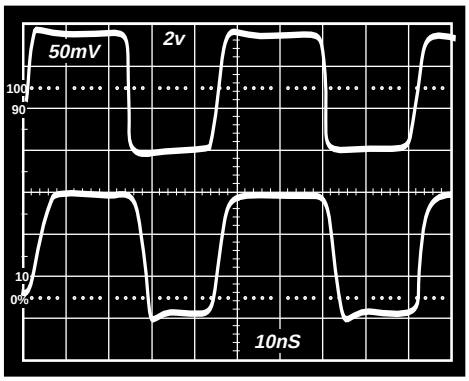


NOTE: $(V_{ANALOG+}) - (V_{ANALOG–}) \geq 3V$

GENERAL DESCRIPTION

The CMP401 and CMP402 are 23 ns and 65 ns quad comparators with separate input and output supplies. Separate supplies enable the input stage to be operated from +3 volts to as high as ±6 volts. The output can be supplied with either +3 volts or +5 volts as determined by the interface logic or available supplies. Independent input and output supplies combined with fast propagation make the CMP401 and CMP402 excellent choices for interfacing to portable instrumentation.

The CMP401 and CMP402 are specified over the extended industrial (–40°C to +125°C) temperature range. Both are available in 16-pin plastic DIP or narrow SO-16 surface mount packages. Consult factory for 16-lead TSSOP availability.



CMP401: 20 MHz Noninverting Switching. V_{IN} = ±100 mV

REV. 0

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

CMP401/CMP402–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ $V+_{ANA}$ = $V+_{DIG}$ = +5.0 V, V_{CM} = 0.1 V, –40°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage[1]	V_{OS}	T_A = +25°C			3	mV
Offset Voltage[1]	V_{OS}				4	mV
Hysteresis				2		mV
Input Bias Current	I_B	T_A = +25°C			3	µA
	I_B				4	µA
Input Offset Current	I_{OS}				±3	µA
Input Common-Mode Voltage Range	V_{CM}		0		+4.0	V
Common-Mode Rejection	CMRR	0.1 V ≤ V_{CM} ≤ 3.9 V	60			dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ		10		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1		µV/°C
OUTPUT CHARACTERISTICS						
Output High Voltage	V_{OH}	I_{OH} = –3.2 mA	4.6			V
Output Low Voltage	V_{OL}	I_{OL} = 3.2 mA			0.2	V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V+_{ANA}$ and $V+_{DIG}$ +2.7 V to +6 V	60			dB
Analog Supply Current – CMP401	I_{ANA}	T_A = +25°C			6.5	mA
Digital Supply Current – CMP401	I_{DIG}	V_O = 0 V, R_L = ∞, T_A = +25°C			2.0	mA
Analog Supply Current – CMP401	I_{ANA}				8.0	mA
Digital Supply Current – CMP401	I_{DIG}	V_O = 0 V, R_L = ∞			2.25	mA
Analog Supply Current – CMP402	I_{ANA}	T_A = +25°C			1.4	mA
Digital Supply Current – CMP402	I_{DIG}	V_O = 0 V, R_L = ∞, T_A = +25°C			2.0	mA
Analog Supply Current – CMP402	I_{ANA}				1.75	mA
Digital Supply Current – CMP402	I_{DIG}	V_O = 0 V, R_L = ∞			2.25	mA
DYNAMIC PERFORMANCE						
Propagation Delay – CMP401	t_P	100 mV Step with 20 mV OD, T_A = +25°C		17	23	ns
Propagation Delay – CMP401	t_P	100 mV Step with 5 mV OD, T_A = +25°C		33		ns
Propagation Delay – CMP401	t_P	100 mV Step with 20 mV OD			30	ns
Propagation Delay – CMP402	t_P	100 mV Step with 20 mV OD, T_A = +25°C		54	65	ns
Propagation Delay – CMP402	t_P	100 mV Step with 5 mV OD, T_A = +25°C		60		ns
Propagation Delay – CMP402	t_P	100 mV Step with 20 mV OD			75	ns

ELECTRICAL SPECIFICATIONS (@ V_{ANA} = V_{DIG} = +3.0 V, V_{CM} = 0.1 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage[1]	V_{OS}				4.5	mV
Input Common-Mode Voltage Range	V_{CM}		0		+2.0	V
Input Differential Voltage Range	V_{DIFF}		±2.0			V
Common-Mode Rejection	CMRR	0.1 V ≤ V_{CM} ≤ 1.9 V	60			dB
OUTPUT CHARACTERISTICS						
Output High Voltage	V_{OH}	I_{OH} = –3.2 mA	2.6			V
Output Low Voltage	V_{OL}	I_{OL} = 3.2 mA			0.25	V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V+_{ANA}$ and $V+_{DIG}$ +2.7 V to +6 V	60			dB
Analog Supply Current – CMP401	I_{ANA}				6	mA
Digital Supply Current – CMP401	I_{DIG}	V_O = 0 V, R_L = ∞			1	mA
Analog Supply Current – CMP402	I_{ANA}				1.2	mA
Digital Supply Current – CMP402	I_{DIG}	V_O = 0 V, R_L = ∞			1	mA
DYNAMIC PERFORMANCE						
Propagation Delay – CMP401	t_P	100 mV Step with 20 mV OD		32		ns
Propagation Delay – CMP402	t_P	100 mV Step with 20 mV OD		70		ns

ELECTRICAL SPECIFICATIONS (@ $V\pm_{ANA}$ = ±5 V, V_{DIG} = +5.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage[1]	V_{OS}	V_{CM} = 0 V			3	mV
Input Common-Mode Voltage Range	V_{CM}		–5.0		+4.0	V
Input Differential Voltage Range	V_{DIFF}		±8.0			V
Common-Mode Rejection	CMRR	–4.9 V ≤ V_{CM} ≤ 3.9 V	60			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1	5	µV/°C
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V\pm_{ANA}$ ±3 V to ±6 V	60			dB
Analog Supply Current – CMP401	I_{ANA}				6.5	mA
Digital Supply Current – CMP401	I_{DIG}	V_O = 0 V, R_L = ∞			2.0	mA
Analog Supply Current – CMP402	I_{ANA}				2.0	mA
Digital Supply Current – CMP402	I_{DIG}	V_O = 0 V, R_L = ∞			2.0	mA
DYNAMIC PERFORMANCE						
Propagation Delay – CMP401	t_P	100 mV Step with 20 mV OD			23	ns
Propagation Delay – CMP402	t_P	100 mV Step with 20 mV OD			65	ns

NOTES
[1]Offset voltage is defined as $(V_{OS+} + V_{OS-})/2$.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Total Analog Supply Voltage . . . . . +16 V
Digital Supply Voltage . . . . . +7 V
Analog Positive Supply—Digital Positive Supply . . . . –200 mV
Input Voltage[2] . . . . . ±7 V
Differential Input Voltage . . . . . ±9 V
Output Short-Circuit Duration to GND . . . . . Indefinite
Storage Temperature Range
P, S, RU Package . . . . . –65°C to +150°C
Operating Temperature Range
CMP401G, CMP402G . . . . . –40°C to +125°C
Junction Temperature Range
P, S, RU Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

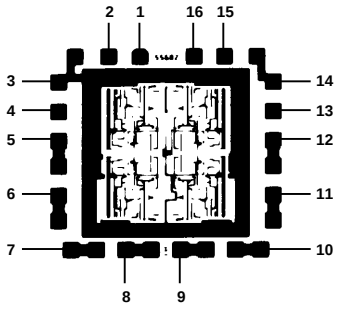
Package Type	θ_{JA}[3]	θ_{JC}	Units
16-Pin Plastic DIP (P)	90	47	°C/W
16-Pin SO (S)	113	37	°C/W
16-Lead TSSOP (RU)	180	37	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]The analog input voltage is equal to ±7 volts or the analog supply voltage, whichever is less.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP, and θ_{JA} is specified for device soldered in circuit board for SOIC and TSSOP packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
CMP401GP	–40°C to +125°C	16-Pin Plastic DIP	N-16
CMP401GS	–40°C to +125°C	16-Pin SOIC	R-16A
CMP401GRU	–40°C to +125°C	16-Lead TSSOP	RU-16
CMP402GP	–40°C to +125°C	16-Pin Plastic DIP	N-16
CMP402GS	–40°C to +125°C	16-Pin SOIC	R-16A
CMP402GRU	–40°C to +125°C	16-Lead TSSOP	RU-16

DICE CHARACTERISTICS



CMP401/CMP402 Die Size 0.065 × 0.069 inch, 4,485 sq. mils
Substrate (Die Backside) Is Connected to V+
Transistor Count 104.

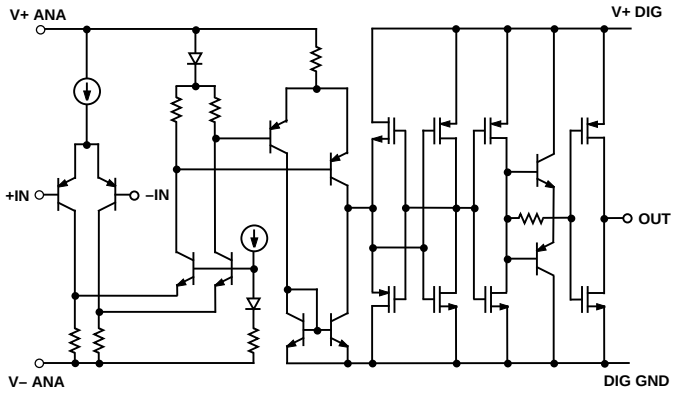
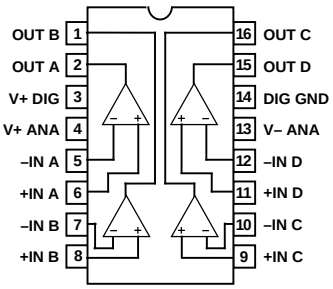


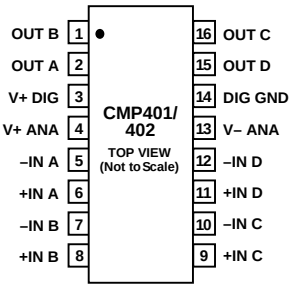
Figure 1. Simplified Schematic

CMP401/CMP402 PIN CONFIGURATIONS

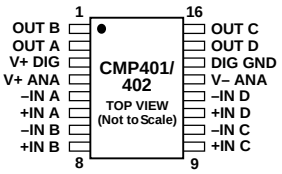
16-Lead Epoxy DIP
(P Suffix)



16-Lead Narrow-SO
(S Suffix)



16-Lead
TSSOP
(RU Suffix)



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the CMP401/CMP402 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

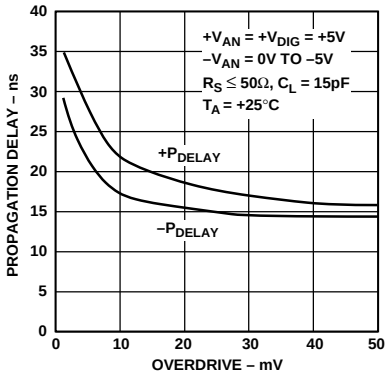


Figure 2. CMP401 Propagation Delay vs. Overdrive

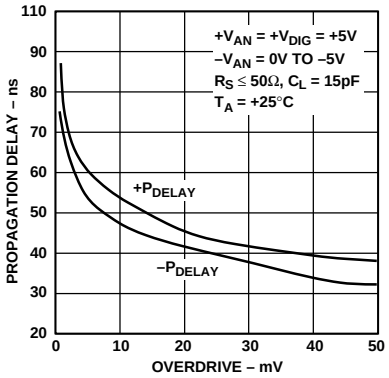


Figure 3. CMP402 Propagation Delay vs. Overdrive

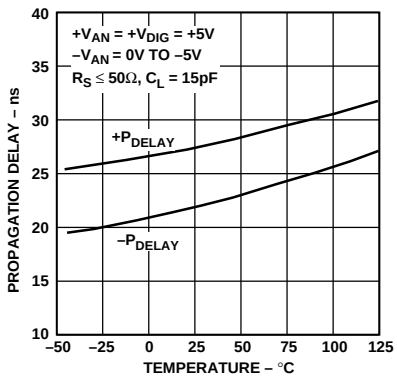


Figure 4. CMP401 Propagation Delay vs. Temperature – 5 mV OD

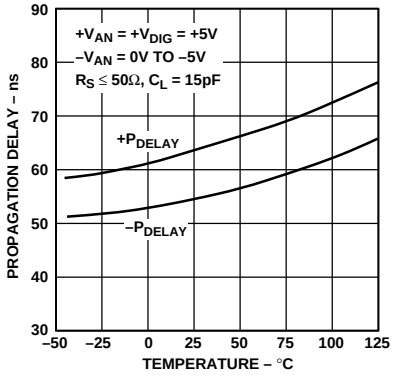


Figure 5. CMP402 Propagation Delay vs. Temperature – 5 mV OD

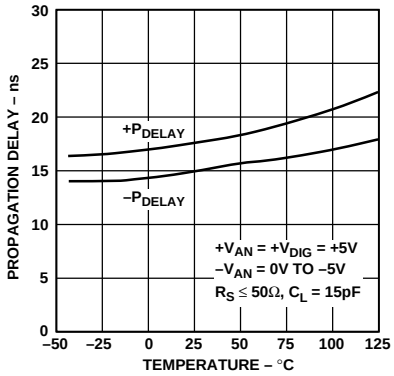


Figure 6. CMP401 Propagation Delay vs. Temperature – 20 mV OD

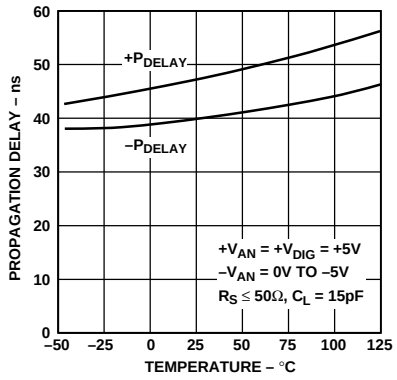


Figure 7. CMP402 Propagation Delay vs. Temperature – 20 mV OD

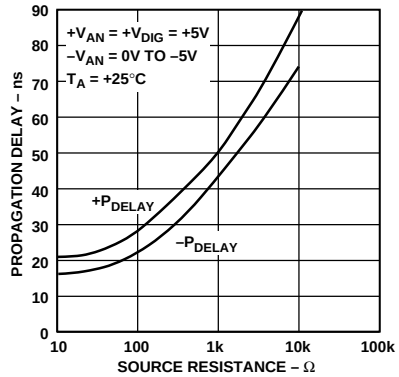


Figure 8. CMP401 Propagation Delay vs. Source Resistance – 20 mV OD

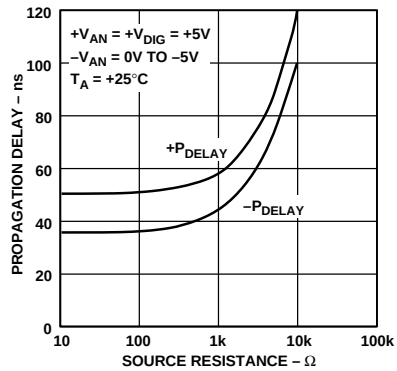


Figure 9. CMP402 Propagation Delay vs. Source Resistance – 20 mV OD

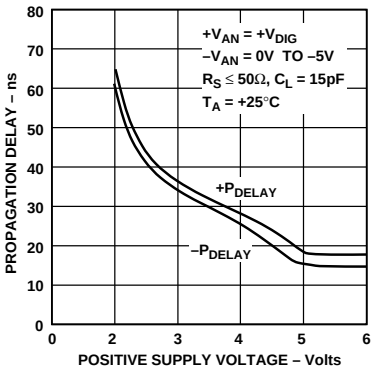


Figure 10. CMP401 Propagation Delay vs. Supply Voltage – 20 mV OD

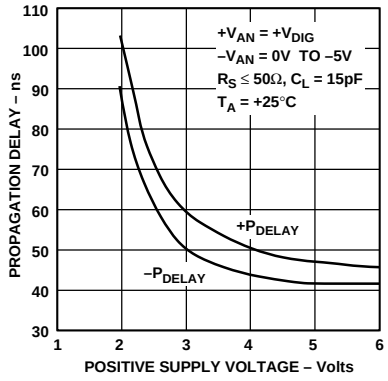


Figure 11. CMP402 Propagation Delay vs. Supply Voltage – 20 mV OD

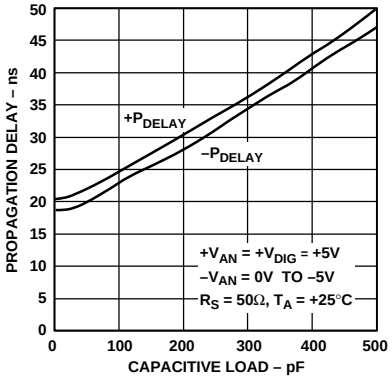


Figure 12. CMP401 Propagation Delay vs. Capacitive Load

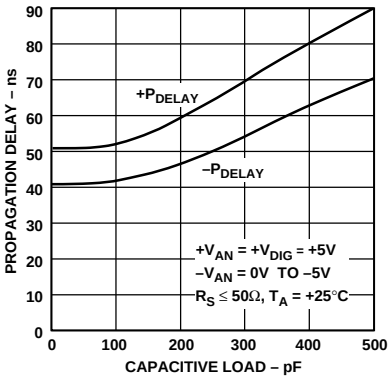


Figure 13. CMP402 Propagation Delay vs. Capacitive Load

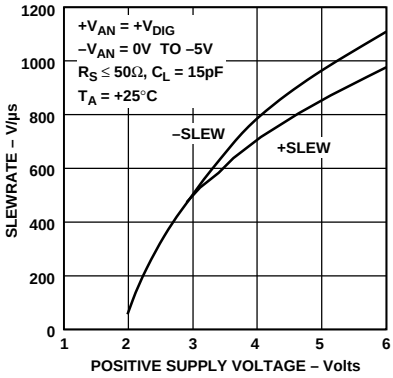


Figure 14. CMP401/CMP402 Slew Rate vs. Positive Supply Voltage

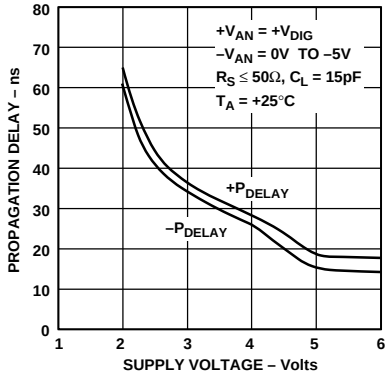


Figure 15. CMP401 Propagation Delay vs. Supply Voltage

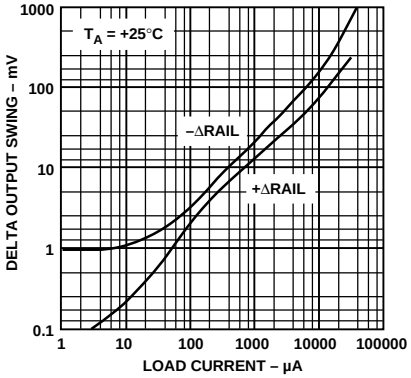


Figure 16. CMP401/CMP402 Delta Output Swing from Power Supplies vs. Load Current

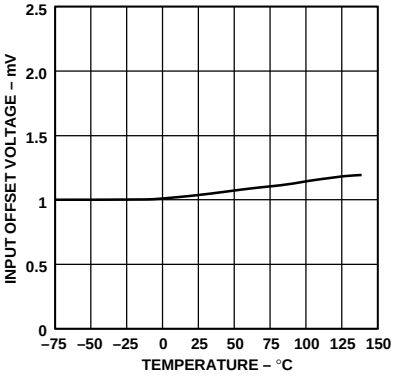


Figure 17. CMP401/CMP402 Input Offset Voltage vs. Temperature

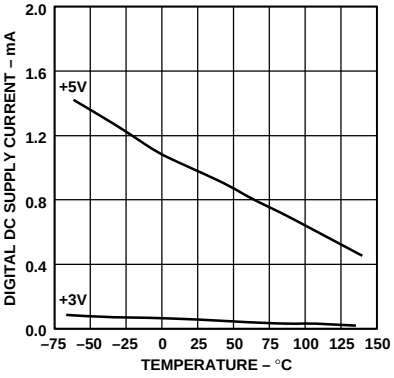


Figure 18. CMP401 Digital Supply Current vs. Temperature

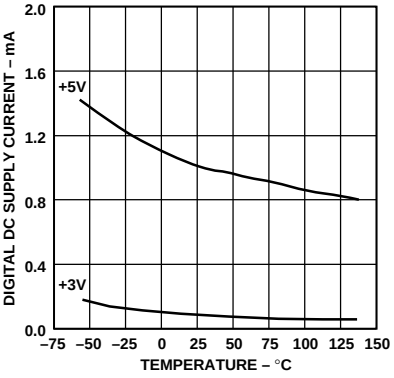


Figure 19. CMP402 Digital Supply Current vs. Temperature

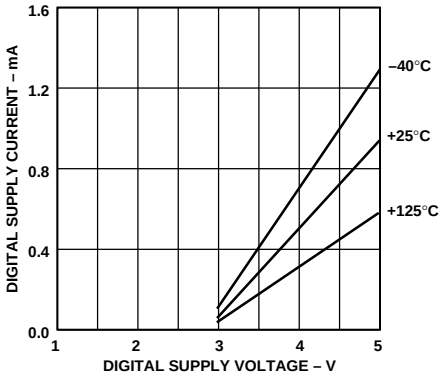


Figure 20. CMP401 Digital Supply Current vs. Digital Supply Voltage

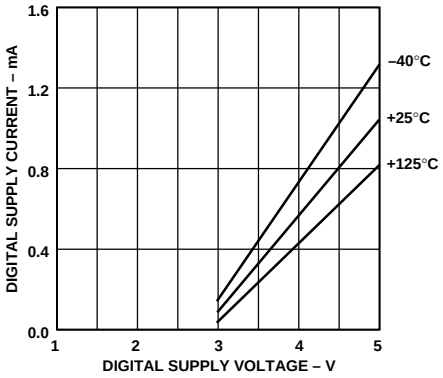


Figure 21. CMP402 Digital Supply Current vs. Digital Supply Voltage

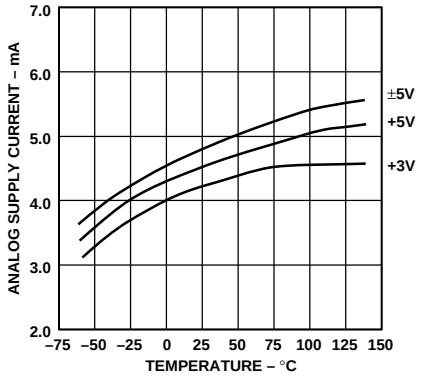


Figure 22. CMP401 Analog Supply Current vs. Temperature

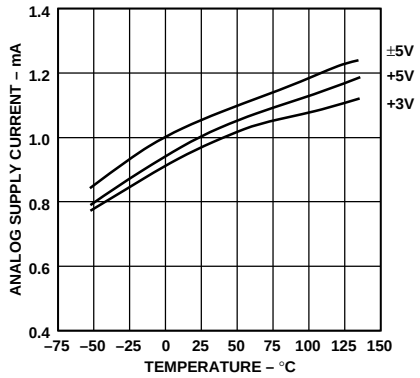


Figure 23. CMP402 Analog Supply Current vs. Temperature

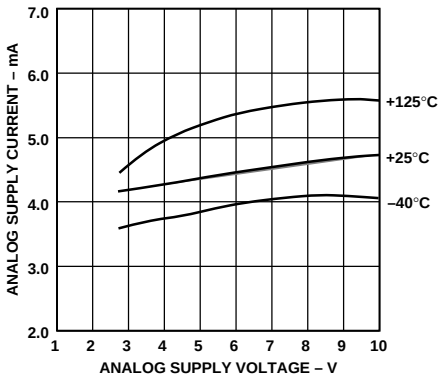


Figure 24. CMP401 Analog Supply Current vs. Analog Supply Voltage

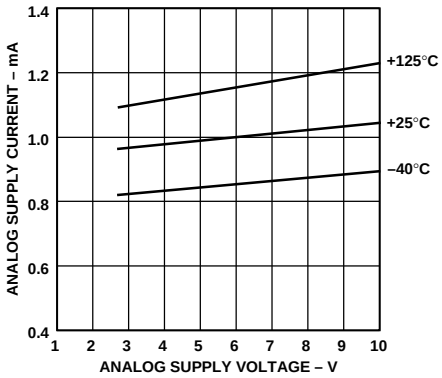
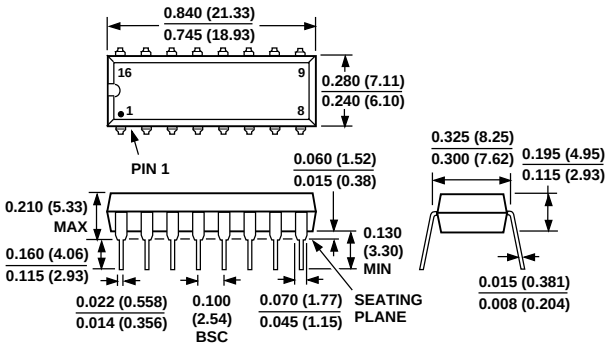


Figure 25. CMP402 Analog Supply Current vs. Analog Supply Voltage

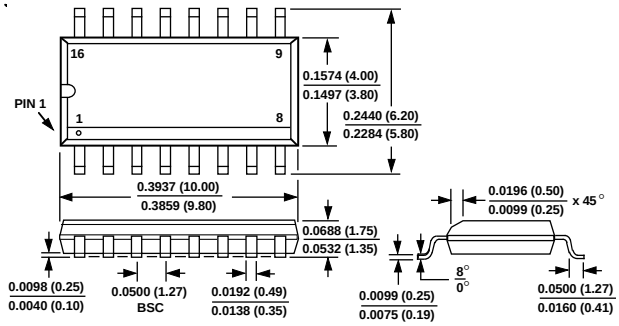
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

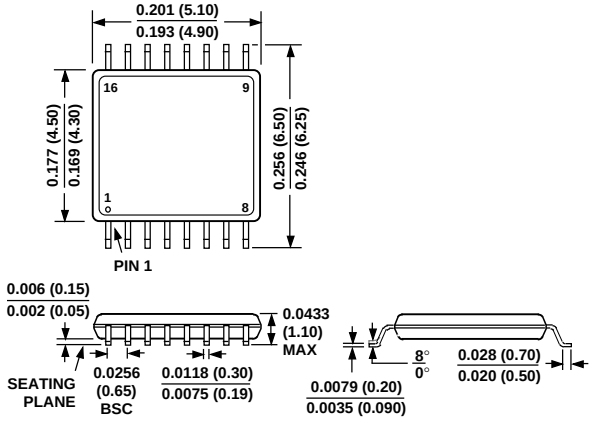
16-Pin Epoxy DIP
(N-16)



16-Pin Narrow-SOIC
(R-16A)



16-Lead TSSOP
(RU-16)



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